**Homework 3**

**Problem Statement:**

**In this assignment, you are to design a circuit that has two input ports: data (8-bit) and reset (1-bit) and one 4-bit output port. After a complete synchronous pulse on reset, in the next eight clocks, the circuit receives eight bytes of data on the data port on every rising edge of clock. There is a module which calculates number of 1s for each received input. The output of this circuit should be maximum number of 1s between all 8 inputs (As the maximum value of output is 8, 4 bits is enough for it).**

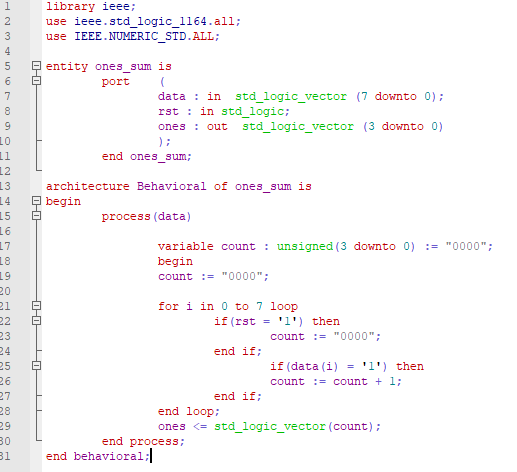
Flow Diagram:



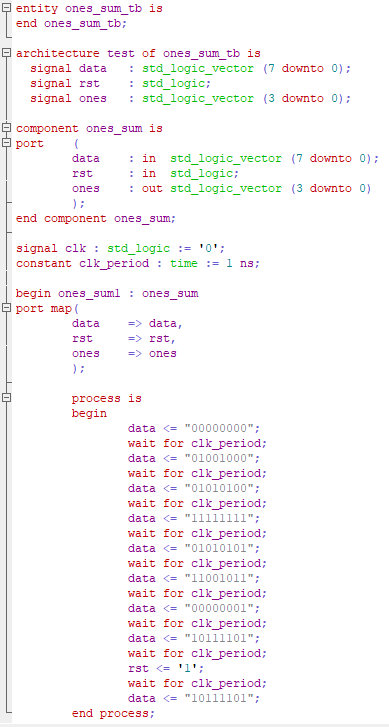
State Diagram:



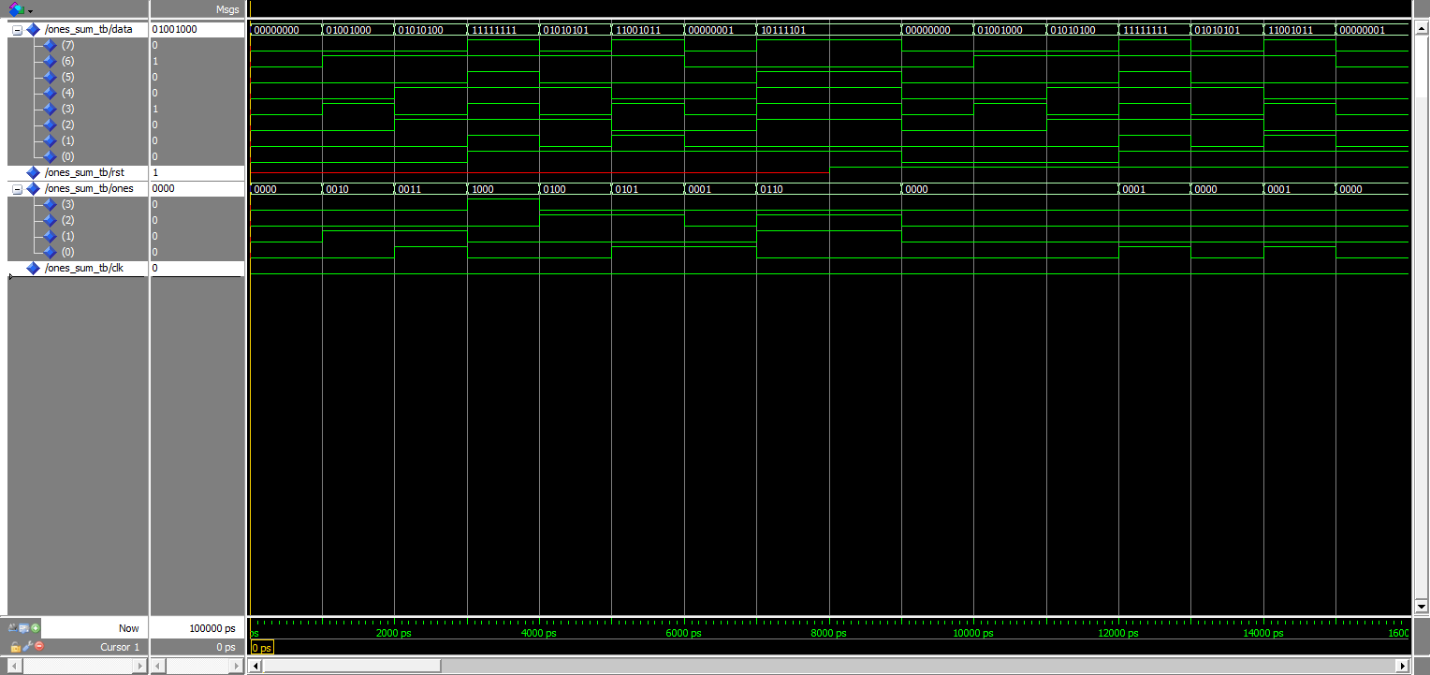
Summing Module:



Test Bench:



Simulation:



Conclusion:

VHDL allowed us to create a complex module with a few lines of code, and easily test the functionality of that code without needing to build in expensive hardware.